FIG.1
Related Art

data line(ramp)

SEL

VDD

VDD

C_s

P1

P0

OEL

FIG.2

data line(ramp)

SEL

VDD

VDD

C_s
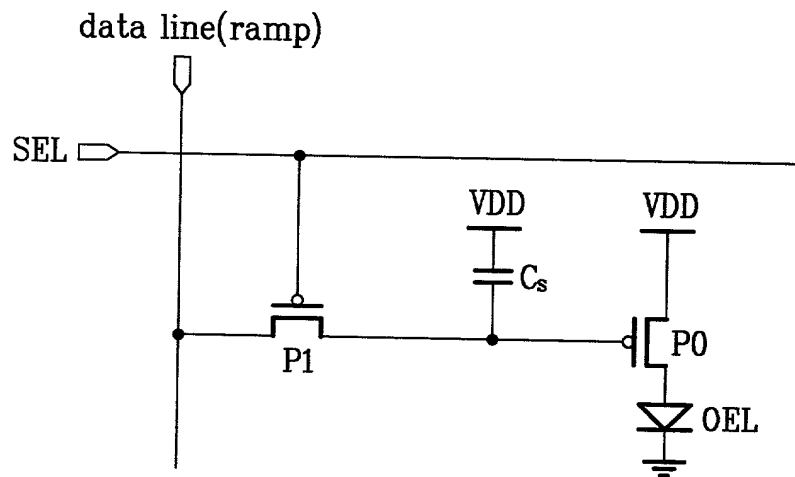
P1

P0

I_{OUT}

SEL1

P2
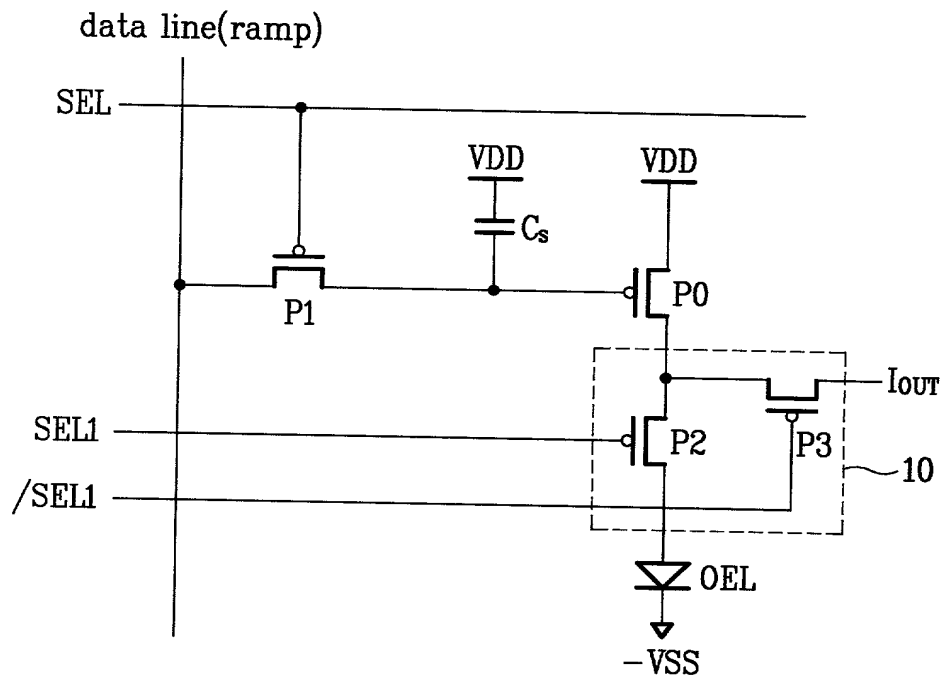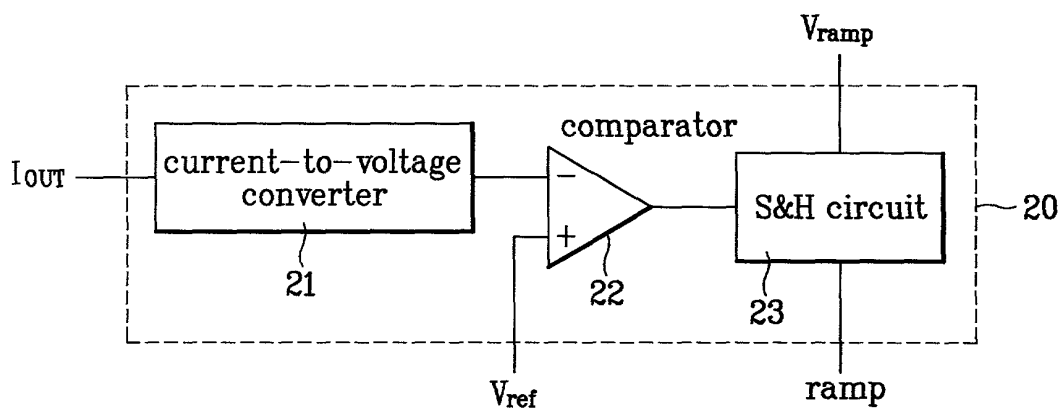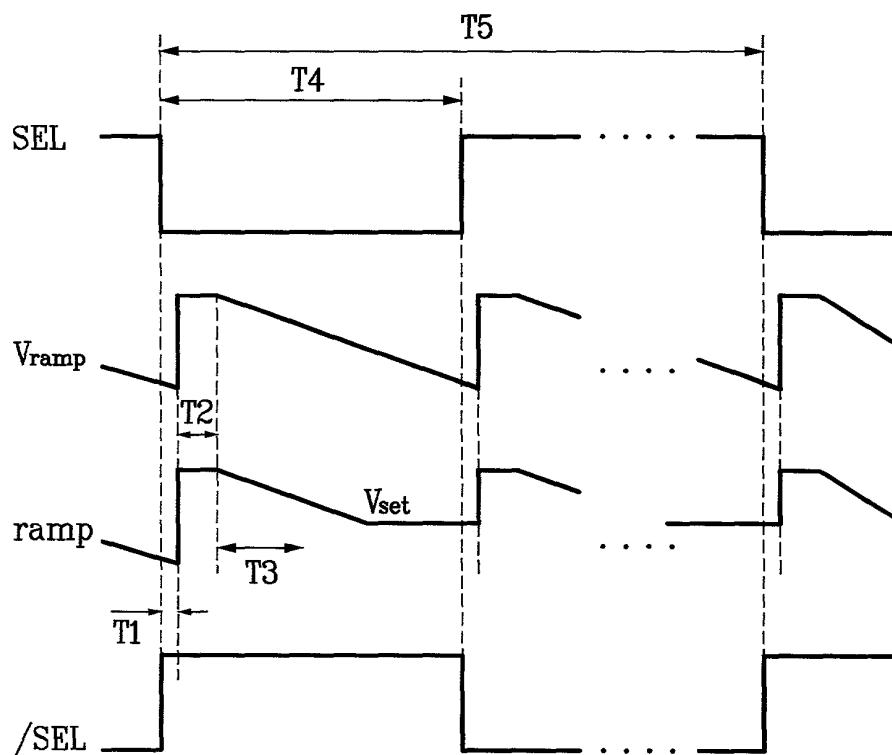
P3

10

/SEL1

OEL

−VSS

FIG.3

FIG.4

T1 : Hold Time
T2 : Data Clear Time
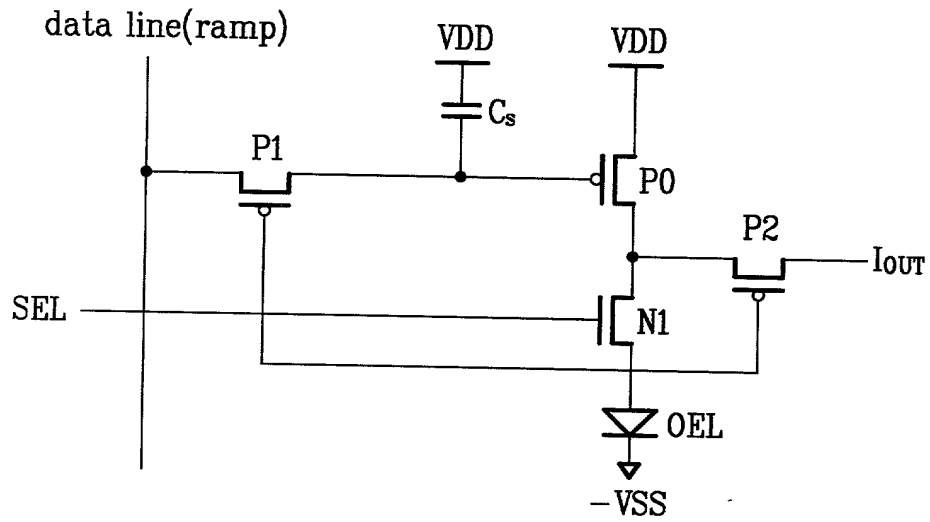T3 : Data Decision Time
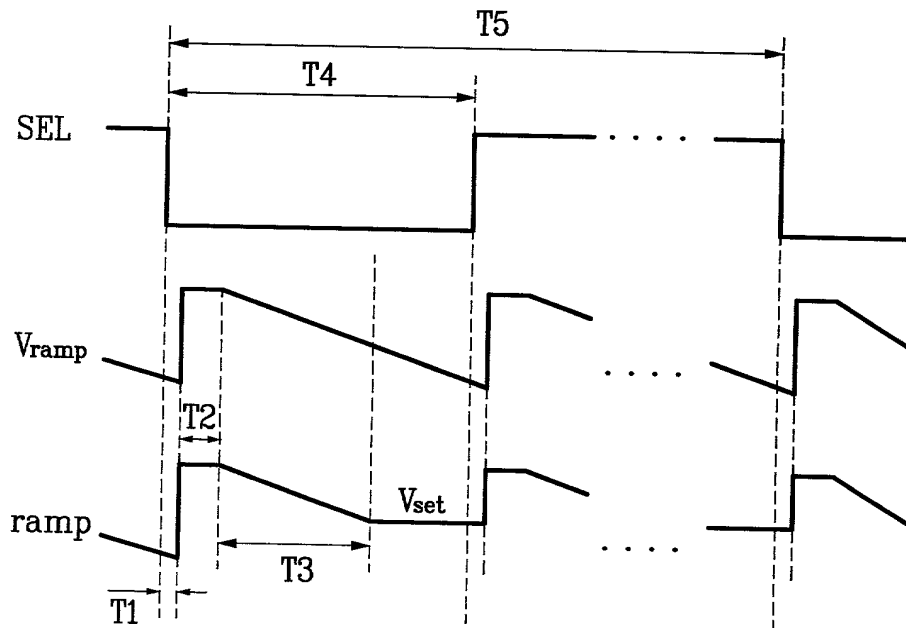T4 : 1 Line Time
T5 : 1 Frame Time

FIG.5

FIG.6

T1 : Hold Time
T2 : Data Clear Time
T3 : Data Decision Time
T4 : 1 Line Time
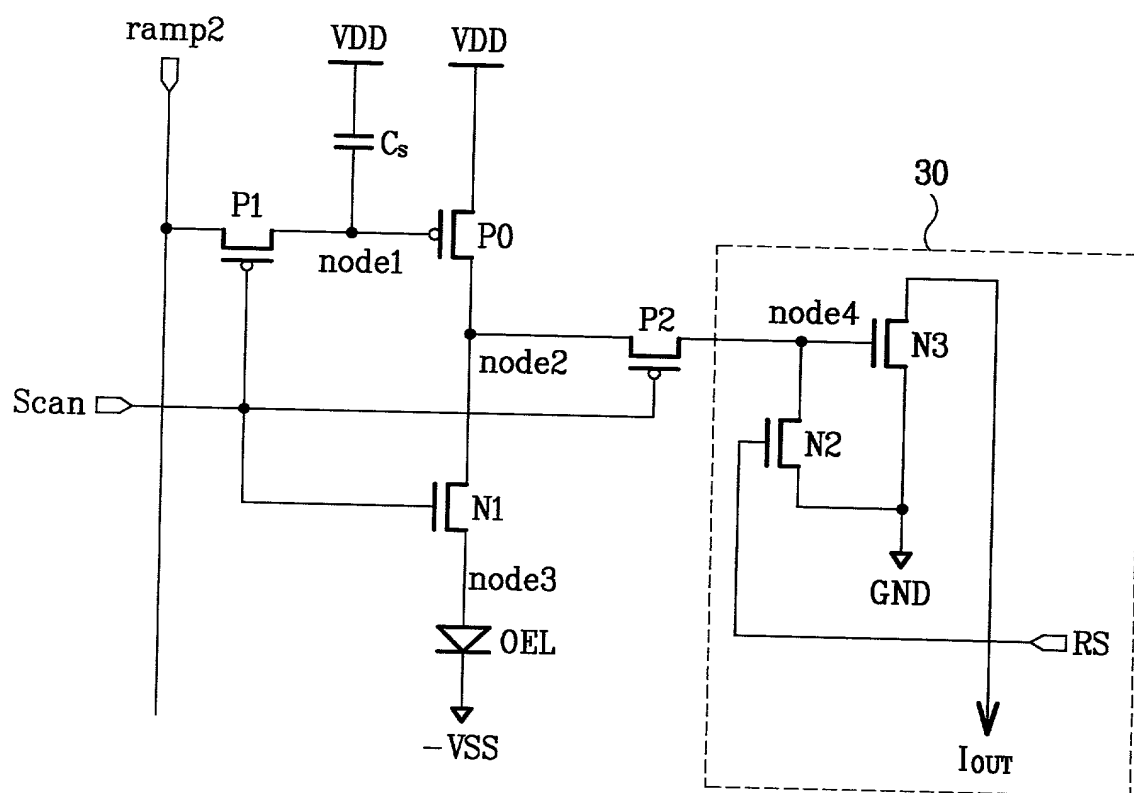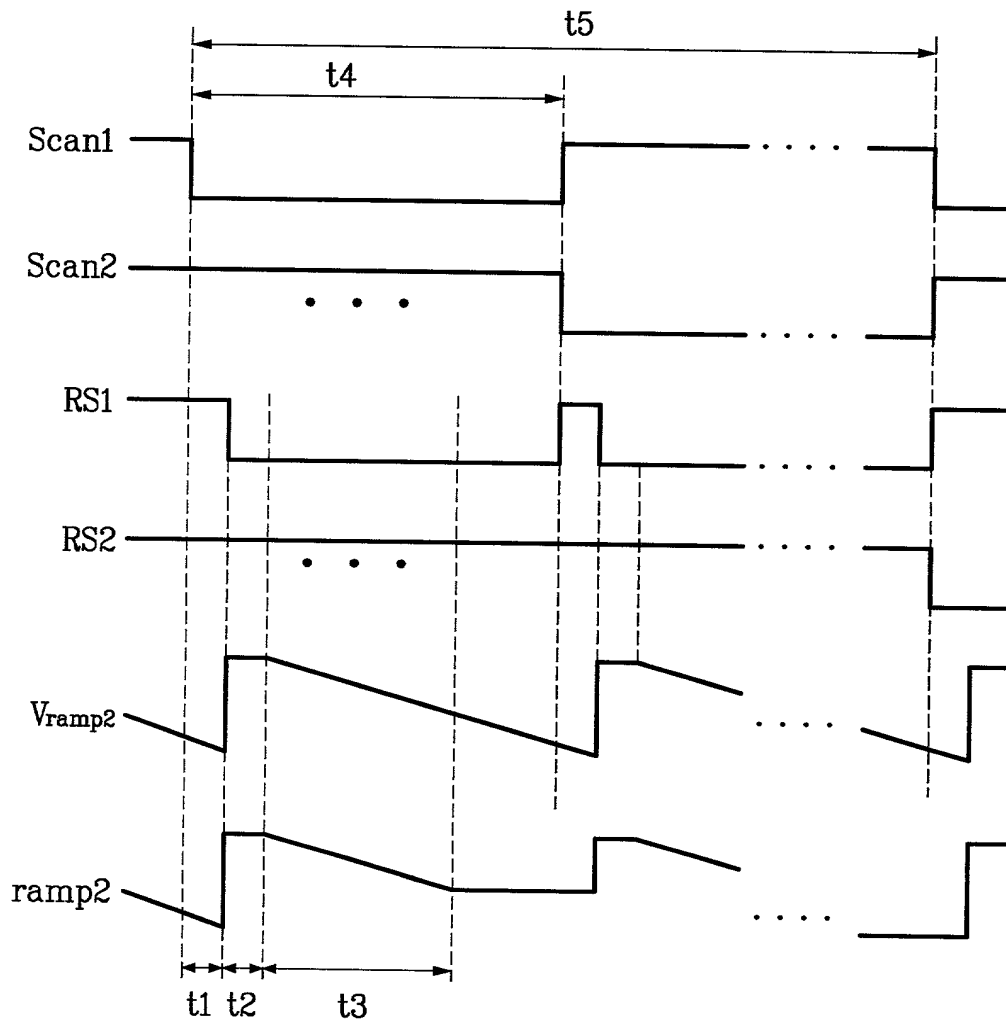T5 : 1 Frame Time

FIG.7

FIG.8

t1 : I_out Reset Time
t2 : Data Reset Time
t3 : Data Writing Time
t4 : One Scan Time
t5 : One Frame Time

FIG.9